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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,886	CADY ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,23-31 and 36-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2,25-27 and 36-54* is/are allowed.

6)☒ Claim(s) *23,24,28,29 and 31* is/are rejected.

7)☒ Claim(s) *30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Amendment filed October 13, 2005 (Certificate of Mailing date: October 11, 2005). The Examiner acknowledges the amendments to the Abstract and claims, the addition of new claims and the submission of the replacement drawings. As a result of the amendments to the claims, Claims 1,2, 23-31, 36-54 are now pending in the instant amended Application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> **The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.**

3. Claim 24 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The Examiner cannot determine the scope of the claim due to the limitation of "a module connective facility" in lines 7-8. First of all, there is no recitation, and there appears to be no supporting explanation, of this limitation in the disclosure. One is left to only imagine what the "module connective facility alludes to in the disclosure. The Examiner cannot now determine whether the limitation does or does not have support in the disclosure without clarification and a change in the

language of the limitation consistent with the support provided for it, if any, in the disclosure.

Claim Objections

4. Claim 24 is objected to because the claim is indefinite for failing to particularly point out and distinctly claim the subject matter with Applicant regards as the invention, as required under 37 CFR § 1.75(a).

The recitation in lines 7-8 of "a module connective facility is indefinite because the concept of a "connective facility" cannot be precisely determined in the context of the claim. What is the "module connective facility" that the consolidated contacts of the second CSP "merge with"? Is it another consolidated contact, perhaps on the first CSP; if so, why is it not so claimed? Is it yet another kind of contact or pad on the first CSP? Is it a contact or pad on another part of the module, not on the first or the second CSP? The Examiner is uncertain of what the Applicant contemplates as "a module connective facility."

5. Appropriate correction is required.

Rejections Based On Prior Art

6. The following rejections were relied upon for the rejections hereinbelow:

Warner et al. (US 2003/0168725 A1)* Isaak (US 6,323,060 B1)*

*Previously made of record in the instant Application.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 23, 24, 28, 29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Warner et al. in view of Isaak.

A) As to Claim 23:

I. Warner et al. discloses: a first microelectronic package 101d; a second microelectronic package 101c, the second microelectronic package 101c disposed above the first microelectronic package 101d (Fig. 3A; paragraph [0043]); flex circuitry 110 (paragraph [0044]) connecting the first microelectronic package 101d and the second microelectronic package 101c, the flex circuitry 110 having plural flex contacts 117 of which at least one has an orifice that has a median opening extent of DO (Fig.

3D; last five lines of paragraph [0046]); plural consolidated contacts 108, a selected one of which passes through the orifice (Fig. 3D) and the selected one of the plural consolidated contacts 108 having an inner flex portion (adjacent microelectronic package 101d and on side 111 of flex circuitry substrate 110) and an outer flex portion (on side 112 of flex circuitry substrate 110; the sides 111 and 112 are not labeled in Fig. 3D but are labeled in Figs. 3B,C and apply to Fig. 3D) delineated by the orifice (Fig. 3D), the selected one of the plural consolidated contacts 108 providing a connection between the first microelectronic package 101d (at pad 103 of package 101d) and the flex circuitry (at pad or via metallization 117; last five lines of paragraph [0046]) and the outer flex portion of consolidated contact 108 having a median lateral extent of DCC and DCC is larger than DO (Fig. 3D).

II. Warner et al. discloses microelectronic packages 101a,b,c,d flip-chip mounted to flex circuitry 110 (paragraph [0044]) but does not disclose packages 101a,b,c,d of a specific type; e.g., chip scale packages. However, Warner et al. further discloses that the microelectronic packages may include a wide variety of chips and packaged chips (paragraph [0042]).

III. Isaak discloses an IC device 104 flip-chip mounted to flex circuitry 102 (Figs. 22 and 25) and arranged in stacked assembly (Fig. 28). Isaak further discloses that the IC device 104 may any one of several types of IC devices including a chip scale package (CSP) (col.4: 1-14).

IV. Since both Warner et al. and Isaak are both in the art of stacked packaging of IC devices by means of flex circuitry and since Isaak discloses that among the

packaged devices that can be stacked in such a manner are CSPs, then the use of CSPs, as taught by Isaak, as the microelectronic packages stacked by means of flex circuitry, in Warner et al., would have been readily recognized as one of the wide variety of IC packages that may be so assembled, as clearly taught in paragraph [0042] in the pertinent art of Warner et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the stacked package assembly of Warner et al. using CSPs as the microelectronic package devices, as taught by Isaak, in order to enhance the functionality of the stacked package of Warner et al. with the high circuit density and compact dimensions of CSPs, as in Isaak.

B) As to Claim 24:

I. Warner et al. discloses a first microelectronic device 101c (Fig. 3A; paragraph [0043]); flex circuitry 110 (paragraph [0044]); a second microelectronic device 101d in stacked relationship with first microelectronic device 101c (Fig. 3A), the second microelectronic device 101d having plural consolidated contacts 108 (Fig. 3D) each of which is one piece of metal (solder; see paragraph [0045]) that has been melted to pass in part through the flex circuitry to merge with "a module connective facility;" –i.e., consolidated contact 108 merges with a pad 214 on the surface 212 of flex circuitry 210 of (paragraph [0045], the last five lines of paragraph [0046] and the first 10 lines of paragraph [0054]), wherein the "merging" is in the form of the usual solder wetting and metal fusion that, in this case occurs on the flex circuitry pad 214 (i.e., the 'connective facility" of the adjacent, lower module 210 in Fig. 4) upon the heating and melting that

forms consolidated solder contact 108 (the embodiment of Fig. 3D) of the first microelectronic device 101c on the upper module 100 in Fig. 4--while providing connection to the flex circuitry (in paragraph [0046], the vias of Fig. 3D are unlined but the pads to which the solder of contact 108 wets are inherently around the via hole on the surfaces 111 and 112 of the flex circuitry substrate 110 and may be among those pads that are connected to leads 115; see the last nine lines of paragraph [0046]).

II. Warner et al. discloses microelectronic packages 101a,b,c,d flip-chip mounted to flex circuitry 110 (paragraph [0044]) but does not disclose packages 101a,b,c,d of a specific type; e.g., chip scale packages. However, Warner et al. further discloses that the microelectronic packages may include a wide variety of chips and packaged chips (paragraph [0042]).

III. Isaak discloses an IC device 104 flip-chip mounted to flex circuitry 102 (Figs. 22 and 25) and arranged in stacked assembly (Fig. 28). Isaak further discloses that the IC device 104 may any one of several types of IC devices including a chip scale package (CSP) (col.4: 1-14).

IV. Since both Warner et al. and Isaak are both in the art of stacked packaging of IC devices by means of flex circuitry and since Isaak discloses that among the packaged devices that can be stacked in such a manner are CSPs, then the use of CSPs, as taught by Isaak, as the microelectronic packages stacked by means of flex circuitry, in Warner et al., would have been readily recognized as one of the wide variety of IC packages that may be so assembled, as clearly taught in paragraph [0042] in the pertinent art of Warner et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the stacked package assembly of Warner et al. using CSPs as the microelectronic package devices, as taught by Isaak, in order to enhance the functionality of the stacked package of Warner et al. with the high circuit density and compact dimensions of CSPs, as in Isaak.

C) As to Claim 28:

I. Warner et al. discloses providing a first microelectronic device 101d having a plurality of ball contacts 108 disposed along a major surface (Figs. 3A and 3D; first two lines of paragraph [0044]); providing flex circuitry 110 (paragraph [0044]) having a plurality of selected flex contacts 117, each penetrated by an orifice (Fig. 3D; first six lines and last five lines of paragraph [0046]); disposing the first microelectronic device 101d proximal to the flex circuitry 110 to place the plurality of ball contacts adjacent to the plurality of flex contacts 117 to pass through the respective orifices to form consolidated contacts each with an inner flex portion and an outer flex portion (Figs. 3A and 3D; paragraph [0044]); applying heat sufficient to melt the plurality of ball contacts (paragraph [0045] teaches that the ball contacts may comprise solder, among other bonding materials); inherently, the step of heating the solder would be required for the ball contacts 108 to pass through the respective orifices to thus form the consolidated contacts each with an inner flex portion and an outer flex portion (as shown in Fig. 3D). [*Examiner's Note*: The inner flex portion is the portion of the resultant melted ball contacts 108 (i.e., consolidated contacts) is the portion of the consolidated contact between the first microelectronic device and 101d and the side 111 of flex circuitry

substrate 110; the outer flex portion of the consolidated contact is the portion of the consolidated contact on the second side 112 of flex circuitry substrate 110 (sides 111 and 112 in Fig. 3D are not labeled but they are labeled in Figs. 3B and 3C, hence apply to Fig. 3D as well)].

II. Warner et al. discloses microelectronic packages 101a,b,c,d flip-chip mounted to flex circuitry 110 (paragraph [0044]) but does not disclose packages 101a,b,c,d of a specific type; e.g., chip scale packages. However, Warner et al. further discloses that the microelectronic packages may include a wide variety of chips and packaged chips (paragraph [0042]).

III. Isaak discloses an IC device 104 flip-chip mounted to flex circuitry 102 (Figs. 22 and 25) and arranged in stacked assembly (Fig. 28). Isaak further discloses that the IC device 104 may any one of several types of IC devices including a chip scale package (CSP) (col.4: 1-14).

IV. Since both Warner et al. and Isaak are both in the art of stacked packaging of IC devices by means of flex circuitry and since Isaak discloses that among the packaged devices that can be stacked in such a manner are CSPs, then the use of CSPs, as taught by Isaak, as the microelectronic packages stacked by means of flex circuitry, in Warner et al., would have been readily recognized as one of the wide variety of IC packages that may be so assembled, as clearly taught in paragraph [0042] in the pertinent art of Warner et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the stacked package assembly of Warner et al.

using CSPs as the microelectronic package devices, as taught by Isaak, in order to enhance the functionality of the stacked package of Warner et al. with the high circuit density and compact dimensions of CSPs, as in Isaak.

D) As to Claim 29, modified Warner et al. further discloses the step of disposing a second microelectronic device (CSP) 101c above first microelectronic device (CSP) 101d (Fig. 3A) and connecting the first and second CSPs with the flex circuitry 110 (Fig. 1 shows the wiring 115 that interconnects the mounting sites 113; see paragraph [0040]).

E) As to Claim 31, modified Warner et al. further discloses that the flex circuitry 110 has two conductive layers (one conductive layer on surface 111, as in Fig. 1, and one conductive layer on surface 112, as in Fig. 2; see paragraph [0040]).

Allowable Subject Matter

10. Claims 1, 2, 25-27 and 36-54 have been allowed.

11. Claim 30 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

12. Applicant's arguments regarding Claims 23, 24, 28-29 and 31 under 35 USC § 103(a) over Warner et al. in view of Isaak, on pp.17-18 of the instant Amendment filed October 13, 2005, have been fully considered but they are not persuasive.

(i) The Applicant directed the Examiner's attention to Fig. 4 and paragraph [0042] of Applicant's supporting disclosure for the description of a "consolidated contact" and believes that no such contact is to be found in Warner et al. The Examiner respectfully disagrees. Fig. 4 and paragraph [0042] of Applicant's supporting disclosure teaches that "*[c]onsolidated contact 61 may be understood to have two portions 61A that may be identified as an 'inner' flex portion and, 61B that may be identified as an 'outer' flex portion, the inner and outer flex portions of consolidated contact 61 being delineated by the orifice. The outer flex portion 61B of consolidated contact 61 has a median lateral extent identified in Fig. 4 as 'DCC' which is greater than the median opening 'DO' of orifice 59.*" Contrary to the Applicant's analysis, the Examiner finds that Fig. 3D does indeed meet the requirements of a "consolidated contact" as described in Fig. 4 and paragraph [0042] of the supporting disclosure and, especially, as recited in the claim language of Claims 23, 24 and 28 by the Applicant. Specifically, in Fig. 3D of Warner et al., which shows an embodiment of contact 108, the "inner flex portion" is the portion of contact 108 that is on the inner side 111 of flex circuitry substrate 110, the "outer flex portion" is on the outer side 112 of flex circuitry substrate 110 (see Figs. 3B,C where sides 111 and 112 on flex circuitry substrate 110 are labeled and which are to be applied to Fig. 3D; see also paragraph [0046] in Warner et al.). The claimed "median lateral extent of DCC" is, in Fig. 3D of Warner et al., a distance defined by the portion of the "outer flex portion" that is larger than the "median opening extent of DO," DO being the diameter of the opening (or "orifice") shown in cross-section in Fig. 3D. Finally, the Examiner notes that the "inner flex portion" and the "outer flex portion" are "delineated

by the orifice," as shown in Fig. 3D. That is, the opening (or, "orifice") in Fig. 3D of Warner et al. defines two portions of the contact 108: one portion ("inner flex portion") above the orifice on surface 111 of flex circuitry substrate 110, and the other portion ("outer flex portion") below the orifice on surface 112 of flex circuitry substrate 110. Therefore, the Fig. 3D embodiment of Warner et al. sufficiently discloses that the contact 108 is every bit as much a "consolidated contact" as is the contact 61 in Fig. 4 and paragraph [0042] of Applicant's disclosure. Accordingly, the Examiner has rejected Claims 23, 24, 28, 29 and 31 over Warner et al. in view of Isaak, which is essentially the same rejection as that given in the Examiner's previous Office Action except with added detail and commentary pointing out the details of the "consolidated contacts" 108 in Warner et al., where necessary.

(ii) Further regarding Claim 24, the Examiner interpreted "a module connective facility" in Warner et al. to be the flex circuitry pad 214 on the adjacent flex circuit 210, with which the consolidated contact 108 of Fig. 3D *merges* (i.e., the solder contact 108 wets and metallically fuses to pad 214) "while providing connection to the flex circuitry," as required by the claim. This interpretation of "a module connective facility" is based on the structural assembly disclosed in Warner et al. in view of the 35 USC § 112 rejection and 37 CFR § 1.75(a) objection to Claim 24 set forth in the present Office Action.

(iii) As to Claim 24, Isaak appears to teach that consolidated contact 106 may be a solder ball–i.e., "one piece of metal"–with flux, in one embodiment (col.10: 1-4), that is melted to even further pass in part through the flex circuitry apertures 118 (col.9: 59-

col.10: 4) but does not appear to teach that the consolidated contact 106, having been thus melted and partially passed through apertures 118 of flex circuitry 102, merges with anything that--at least at this time (i.e., in view of the 35 USC § 112 rejection and objection under 37 CFR § 1.75(a), as set forth in the present Office Action)--can be fairly interpreted in Isaak as "a module connective facility" while providing connection to flex circuitry 102.

(iv) As to Claim 28, Isaak does not teach or fairly suggest that the consolidated contacts 106 that are partially passed in apertures 118 (col.9: 59-col.10: 4) have a structure that comprises an "inner flex portion" and an "outer flex portion," as required by Claim 28.

(v) Accordingly, in view of (iii) and (iv), above, the Claim 28 and, tentatively, the problematic Claim 24, as amended, appear to now distinguish over Isaac.

(vi) Finally, the Examiner notes an error in the Applicant's statement of allowable subject matter in new Claim 39. On p.19, line 1 of the instant Amendment, "8" should read as --9--; i.e., p.19, lines 1-3 should read "[n]ew claim 39 corresponds to original claims 3 and **9** and Applicants note that they interpreted the Examiner's comments on allowability to indicate that claim 8 did not appear to contribute to patentability one way or the other" (bold/underlined correction emphasis, added).

Conclusion

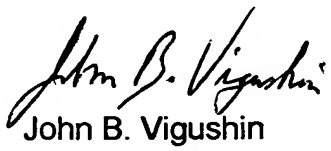
13. Since the Examiner is now raising the issue of 35 USC § 112, 1st paragraph and 37 CFR § 1.75(a) regarding the limitation "a module connective facility," as presented in

Claim 24, as originally filed, the Examiner has made the present Office Action NON-FINAL.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
December 16, 2005